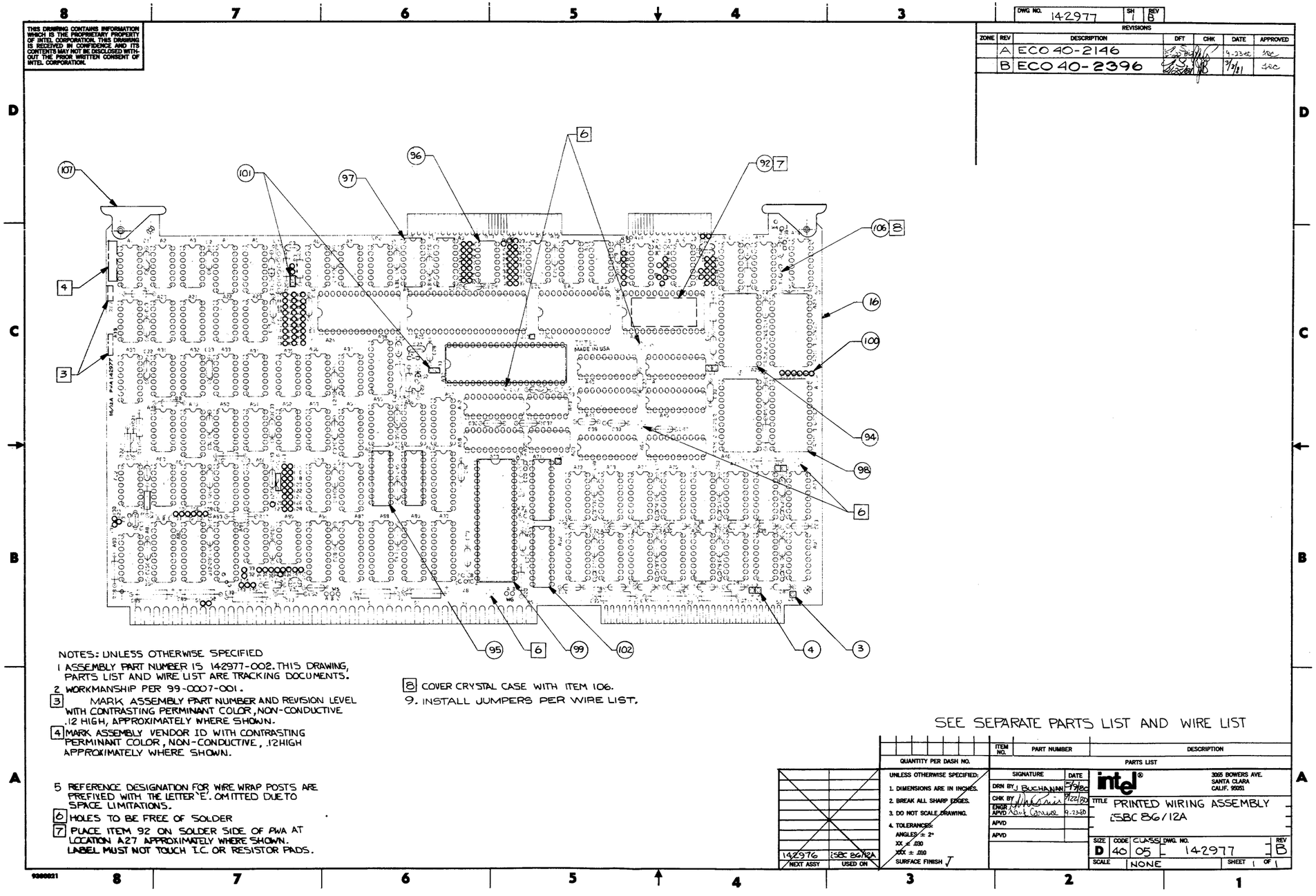
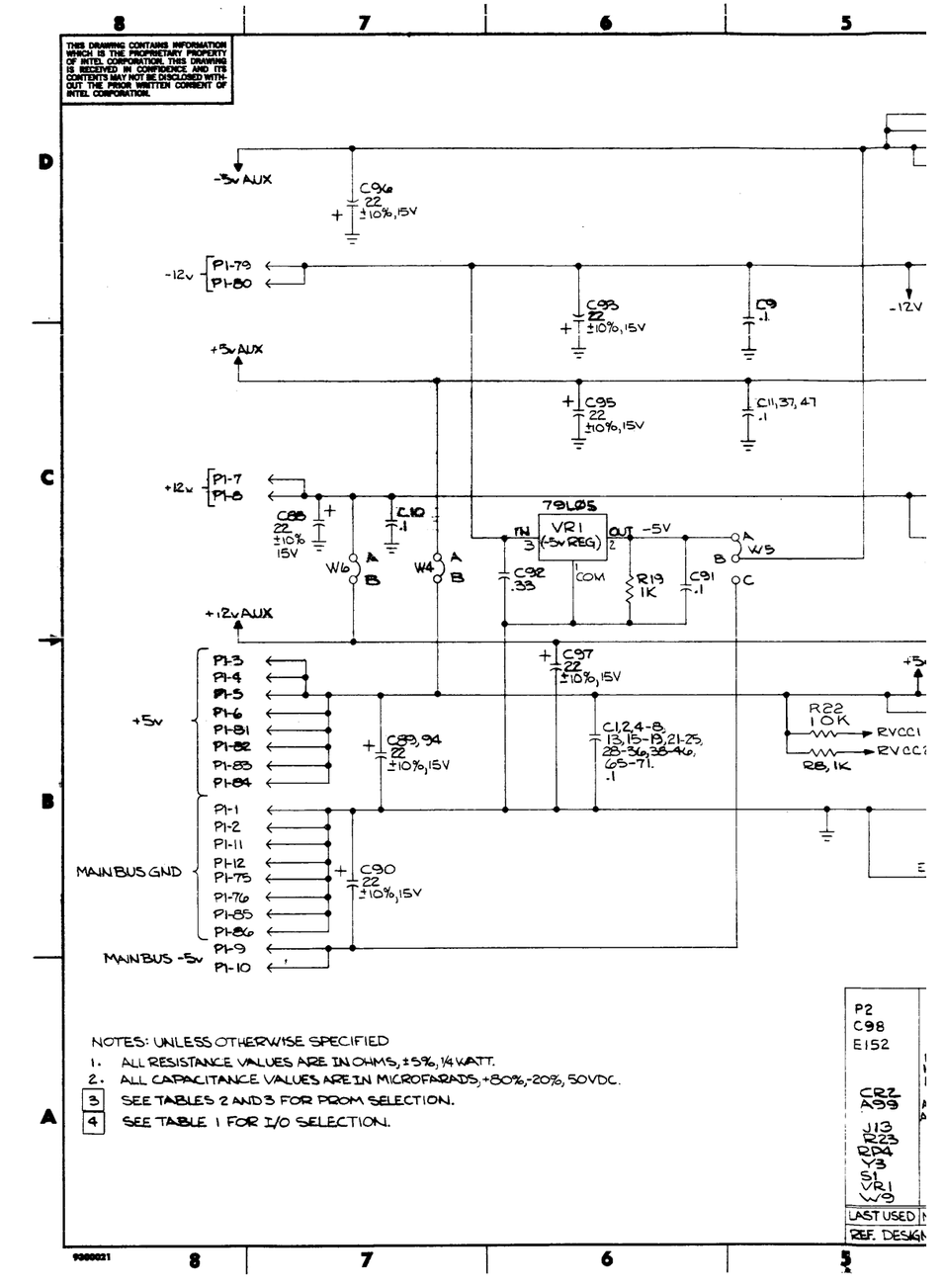


Figure 5-1. iSBC 86/12A Parts Location Diagram

Jumpers

Jumpers	Factory Default	Option
W1	A–B	N/A
W2	A–B	N/A
W3	A–B	N/A
W4	A–B	See table 2-4
W5	A–B	See table 2-4
W6	A–B	See table 2-4
E63-E64	Open	When installed enables common ground between chassis.



Option
N/A
N/A
N/A
table 2-4
d enables common etween chassis.

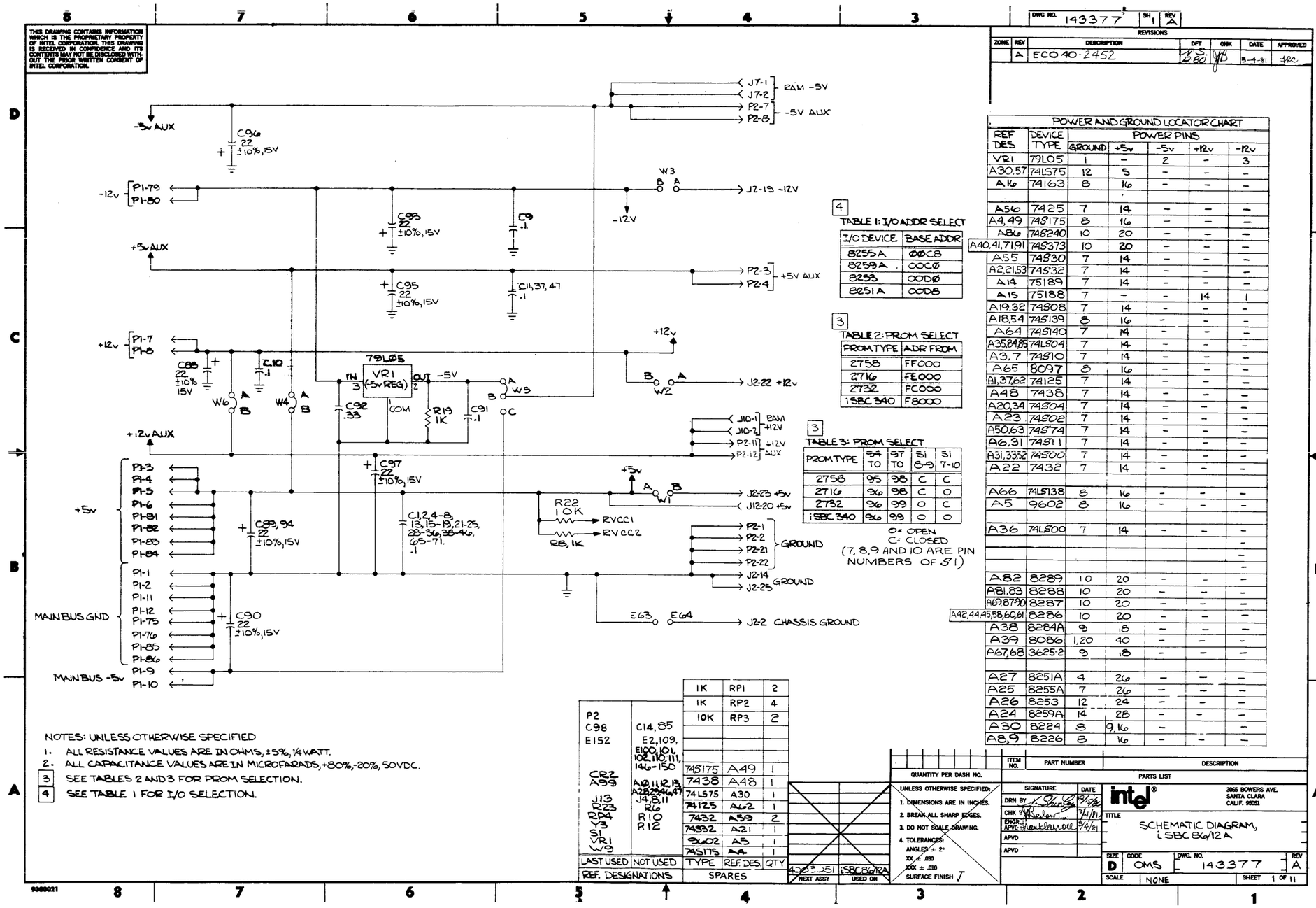


TABLE 1: I/O ADDR SELECT (4)

I/O DEVICE	BASE ADDR
8255A	ØØC8
8259A	ØØCØ
8253	ØØDØ
8251A	ØØD8

TABLE 2: PROM SELECT (3)

PROM TYPE	ADR FROM
2758	FF000
2716	FE000
2732	FC000
iSBC 340	F8000

TABLE 3: PROM SELECT (3)

PROM TYPE	94 TO	97 TO	SI 8-9	SI 7-10
2758	95	98	C	C
2716	96	98	C	O
2732	96	99	O	C
iSBC 340	96	99	O	O

O= OPEN
C= CLOSED
(7, 8, 9 AND 10 ARE PIN NUMBERS OF S1)

POWER AND GROUND LOCATOR CHART

REF DES	DEVICE TYPE	POWER PINS GROUND	+5v	-5v	+12v	-12v
VR1	79L05	1	–	2	–	3
A30,57	74LS75	12	5	–	–	–
A16	74163	8	16	–	–	–
A56	7425	7	14	–	–	–
A4,49	74S175	8	16	–	–	–
A86	748240	10	20	–	–	–
A40,41,71,91	74S373	10	20	–	–	–
A55	74S30	7	14	–	–	–
A2,21,53	74S32	7	14	–	–	–
A14	75189	7	14	–	–	–
A15	75188	7	–	–	14	1
A19,32	74S08	7	14	–	–	–
A18,54	74S139	8	16	–	–	–
A64	74S140	7	14	–	–	–
A35,84,85	74LS04	7	14	–	–	–
A3,7	74S10	7	14	–	–	–
A65	8097	8	16	–	–	–
A1,37,62	74125	7	14	–	–	–
A48	7438	7	14	–	–	–
A20,34	74S04	7	14	–	–	–
A23	74S02	7	14	–	–	–
A50,63	74S74	7	14	–	–	–
A6,31	74S11	7	14	–	–	–
A31,33,52	74S00	7	14	–	–	–
A22	7432	7	14	–	–	–
A66	74LS138	8	16	–	–	–
A5	9602	8	16	–	–	–
A36	74LS00	7	14	–	–	–
						–
						–
						–
A82	8289	10	20	–	–	–
A81,83	8288	10	20	–	–	–
A69,87,90	8287	10	20	–	–	–
A42,44,45,58,60,61	8286	10	20	–	–	–
A38	8284A	9	18	–	–	–
A39	8086	1,20	40	–	–	–
A67,68	3625-2	9	18	–	–	–
A27	8251A	4	26	–	–	–
A25	8255A	7	26	–	–	–
A26	8253	12	24	–	–	–
A24	8259A	14	28	–	–	–
A30	8224	8	9,16	–	–	–
A8,9	8226	8	16	–	–	–

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

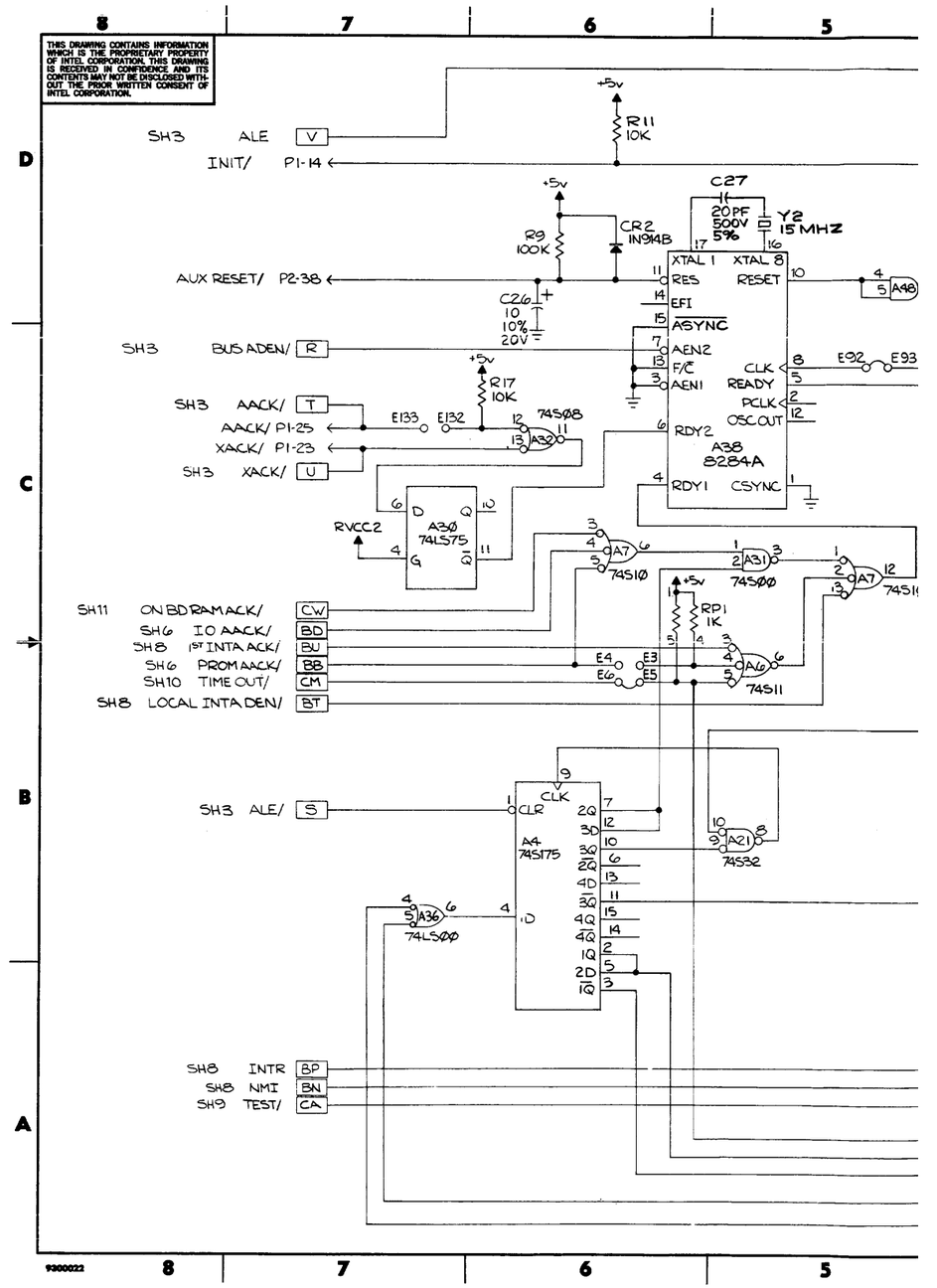
Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 1 of 11)

Jumpers

Jumpers	Factory Default	Option
E3-E4	Open	See table 2-4
E5-E6	Installed	See table 2-4
E92-E93	Installed	N/A
E132-E133	Open	Install to allow use of AACK/ from Multibus interface.

Glossary

AB0-AB13	Address Bus 0-13
AD0-ADF	Address Bits 0-F
ADV IO ADR	Advance Input/Output Address
AUX RESET	Auxiliary Reset
BHE	Byte High Enable
CLK	Clock
INIT	Initialize
LOCK	Lock
RESET	Reset
S0	Status Bit zero
S1	Status Bit one
S2	Status Bit two
SYS CLOCK	System Clock
T21	Timing Pulse 21
TIME OUT INTR	Time Out Interrupt



Option
table 2-4
table 2-4
N/A
ow use of AACK/
ibus interface.

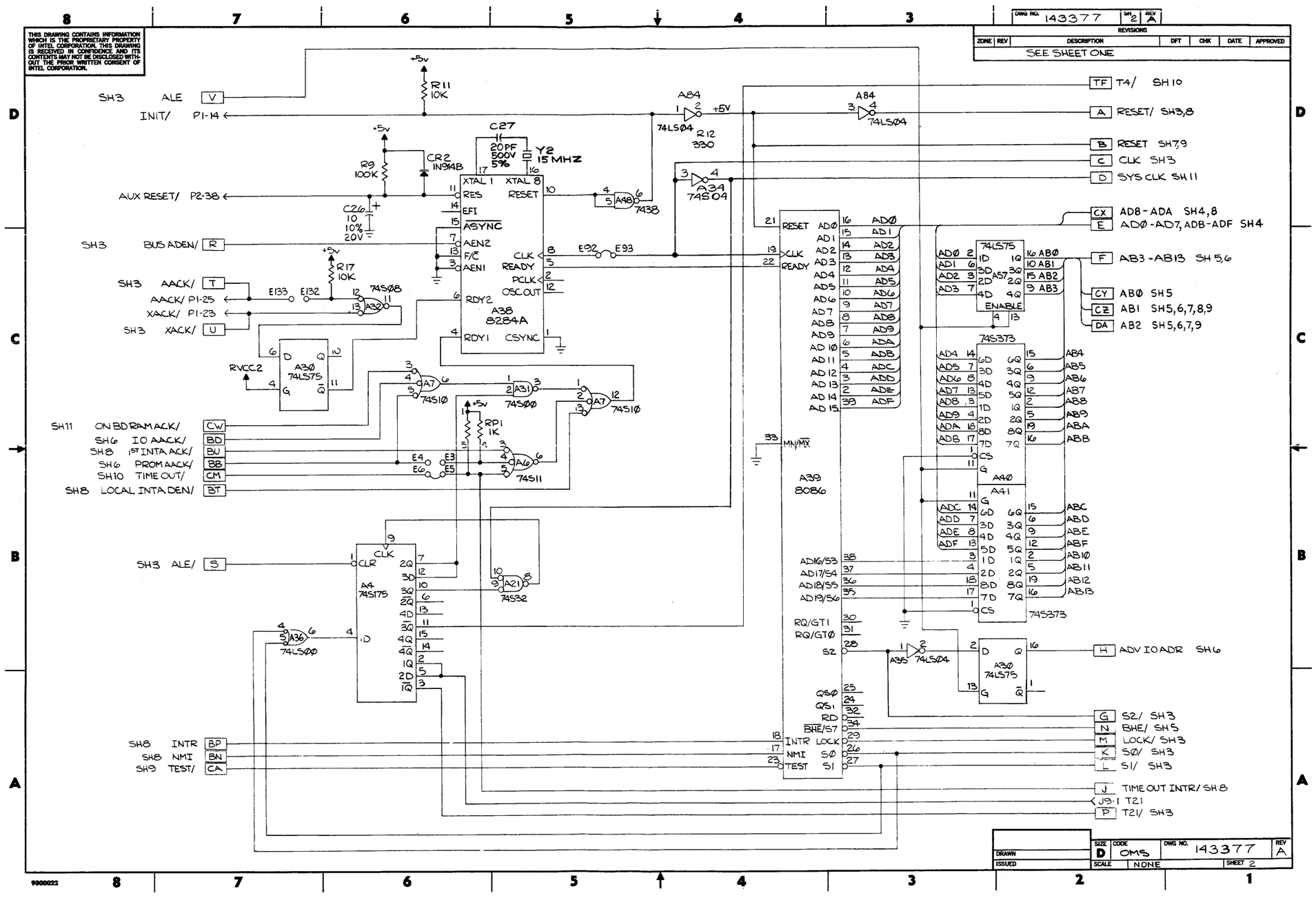


Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 2 of 11)

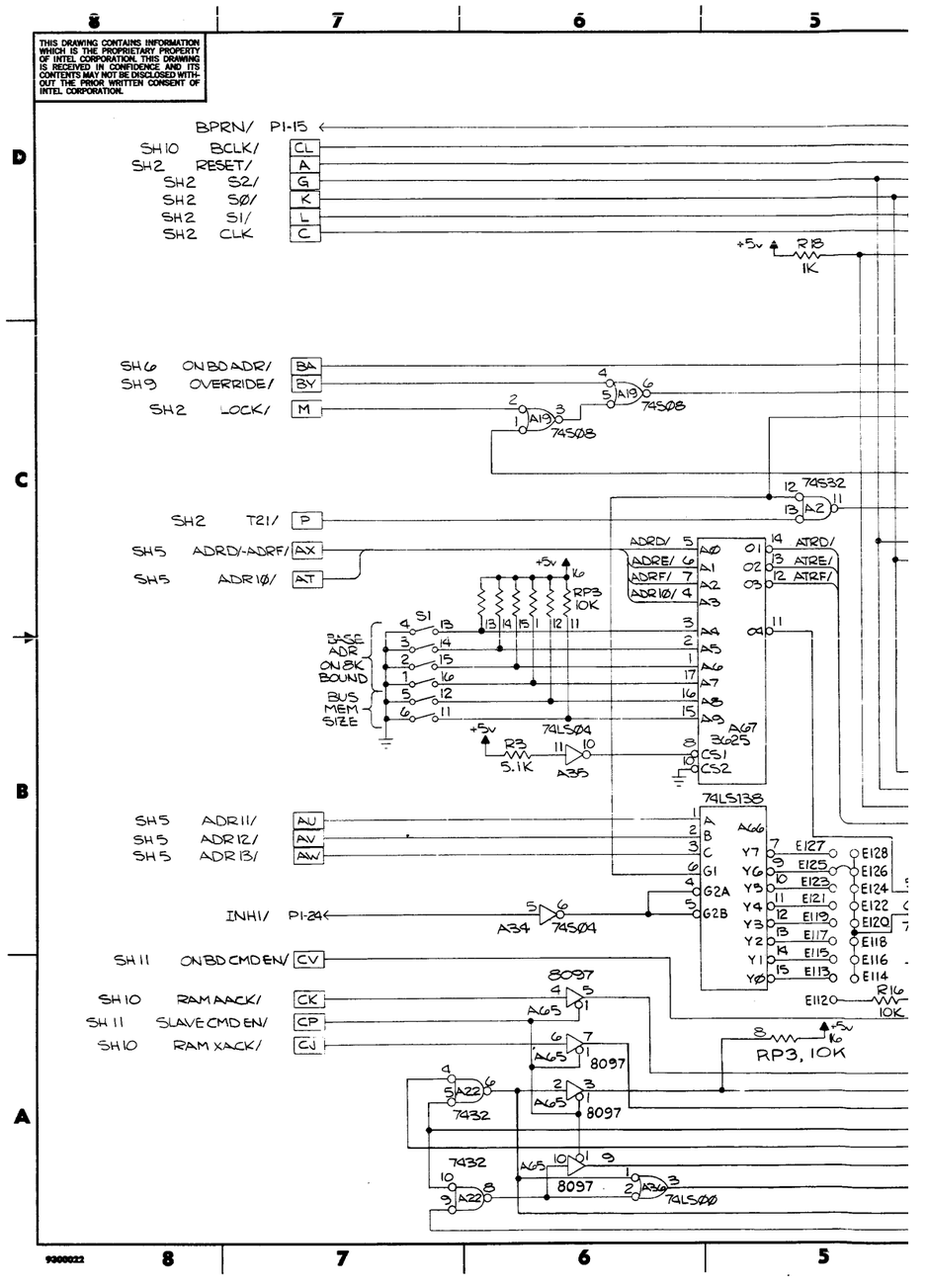
CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Jumpers

Jumpers	Factory Default	Option
E107-E108	Open	Install to use AACK
E112 through E128	E125-E126	See figure 2-1
E129-E130-E131	E129-E130	See table 2-13
E143-E144-E145	E144-E143	See table 2-13
E151-E152	Installed	See paragraph 2-24
W7 A-B-C	A-C	N/A
S1	None	See figure 2-1

Glossary

AACK	Advance Acknowledge
ADV MEM WRT	Advance Memory Write
ALE	Address Latch Enable
ATRD-ATRF	Address Transformed D-F
BPRO	Bus Priority Out
BPRN	Bus Priority In
BREQ	Bus Request
BUS ADEN	Bus Address Enable
BUS DEN	Bus Data Enable
BUSY	Busy
CBRQ	Common Bus Request
DEN	Data Enable
DPRD	Dual Port Read
DPWT	Dual Port Write
DT/$\overline{R}$	Data Transmit/Read
INHI	Inhibit
INTA	Interrupt Acknowledge
INTA CYCLE	Interrupt Acknowledge Cycle
IORC	Input/Output Read Command
IORD	Input/Output Read
IOWC	Input/Output Write Command
IOWT	Input/Output Write
MEM RD	Memory Read
MRDC	Memory Read Command
MWTC	Memory Write Command
OFF BD RAM ADDR REQ	Off Board Random Access Memory Address Request
OFF BD RAM CMD	Off Board Random Access Memory Command
OFF BD RD	Off Board Read
QMCE	Qualified Master Cascade Enable
XACK	Transfer Acknowledge



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use AACK
igure 2-1
able 2-13
able 2-13
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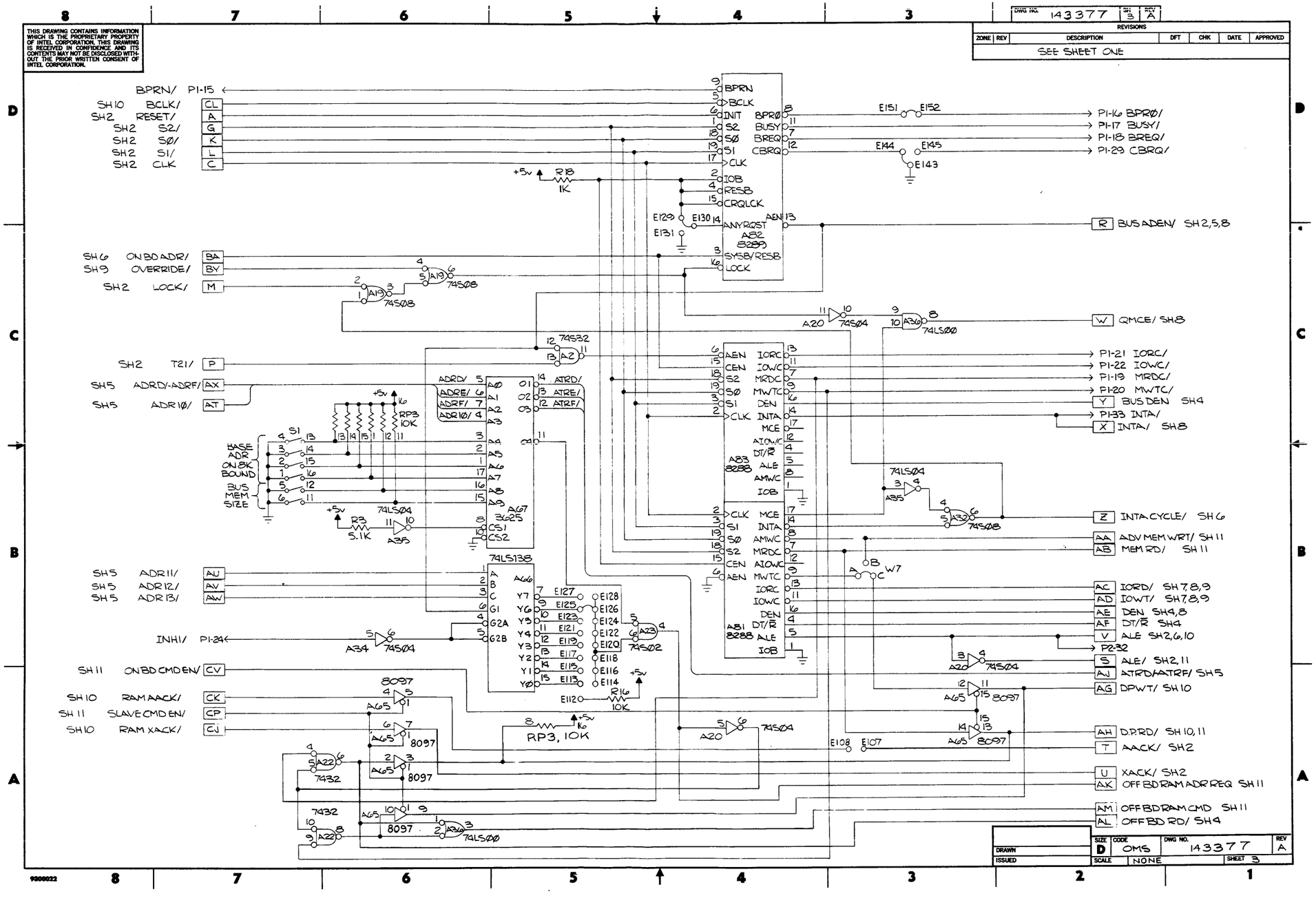
N/A
igure 2-1

est

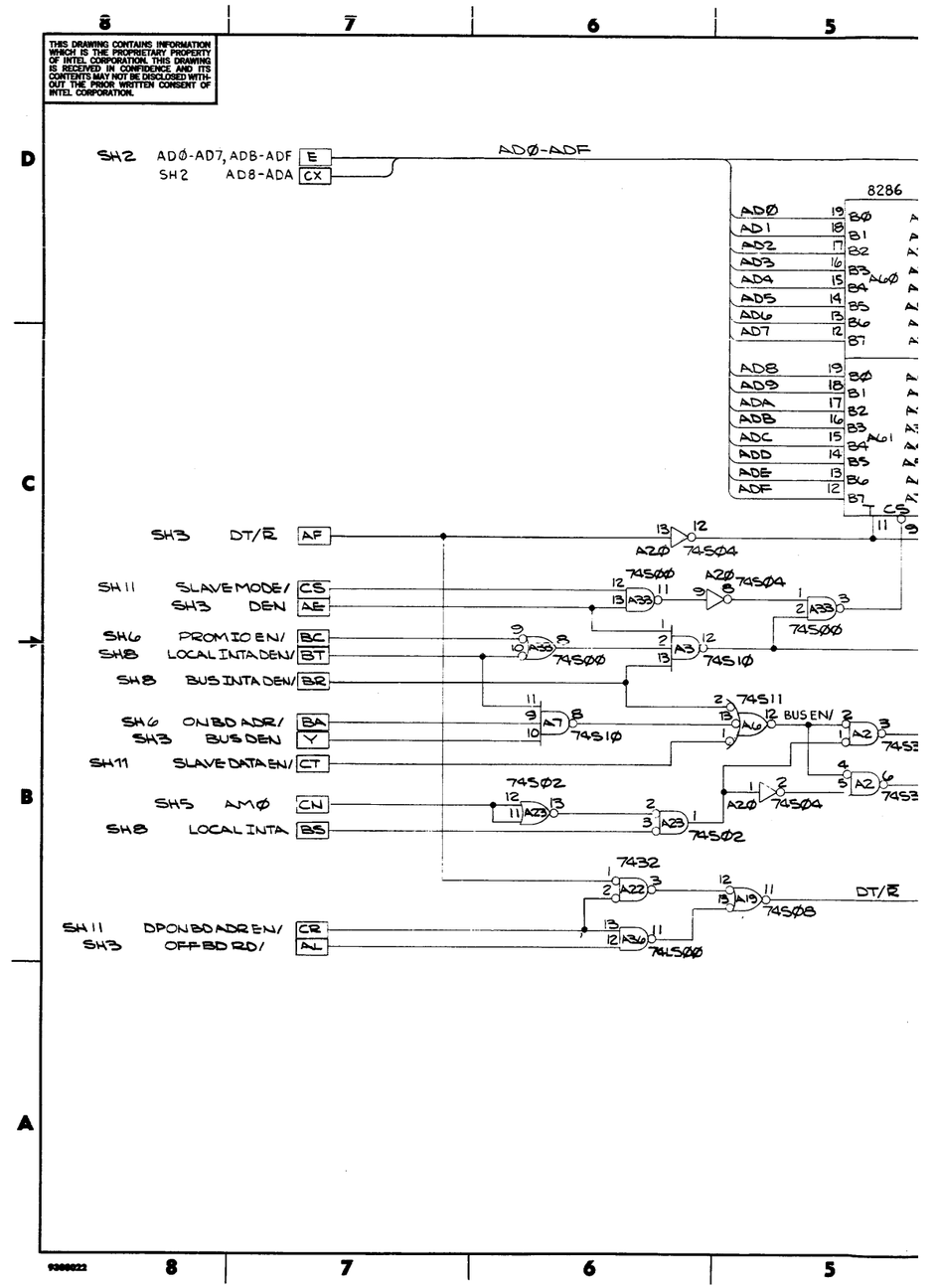


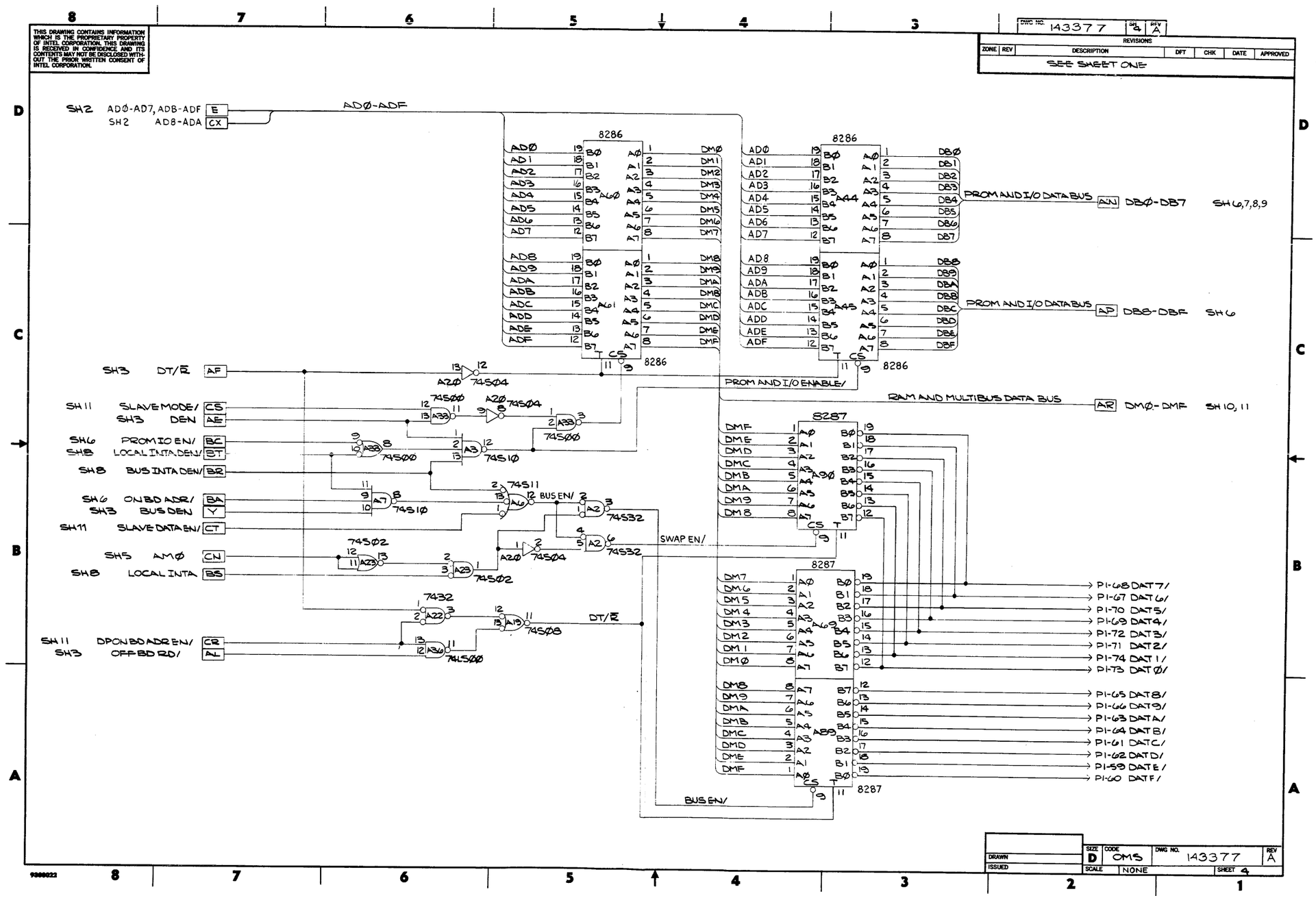
CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 3 of 11)

Glossary

DAT0-DATF	Data Bits 0-F
DB0-DBF	Data Bus 0-F
DM0-DMF	Multibus Data 0-F



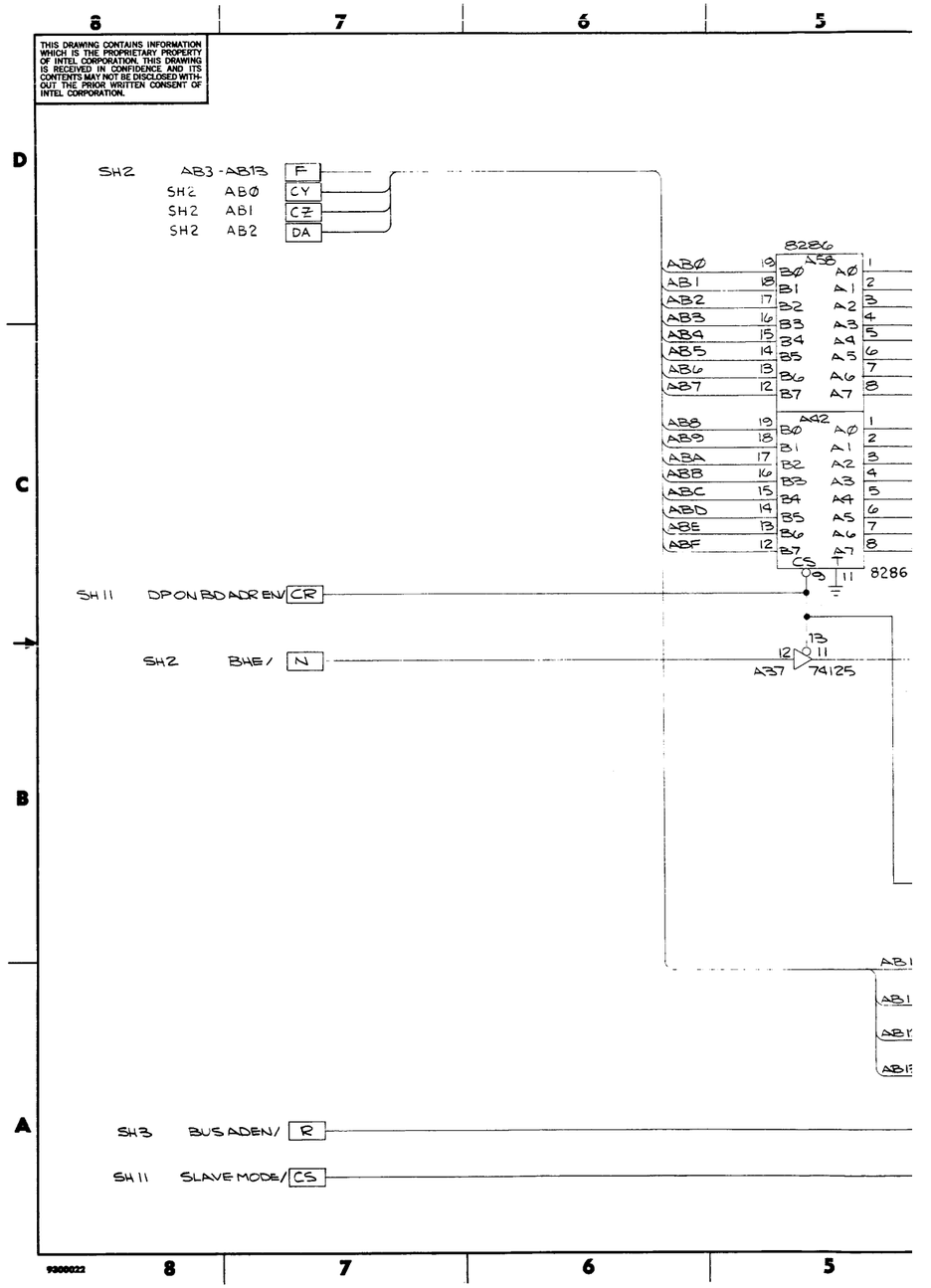


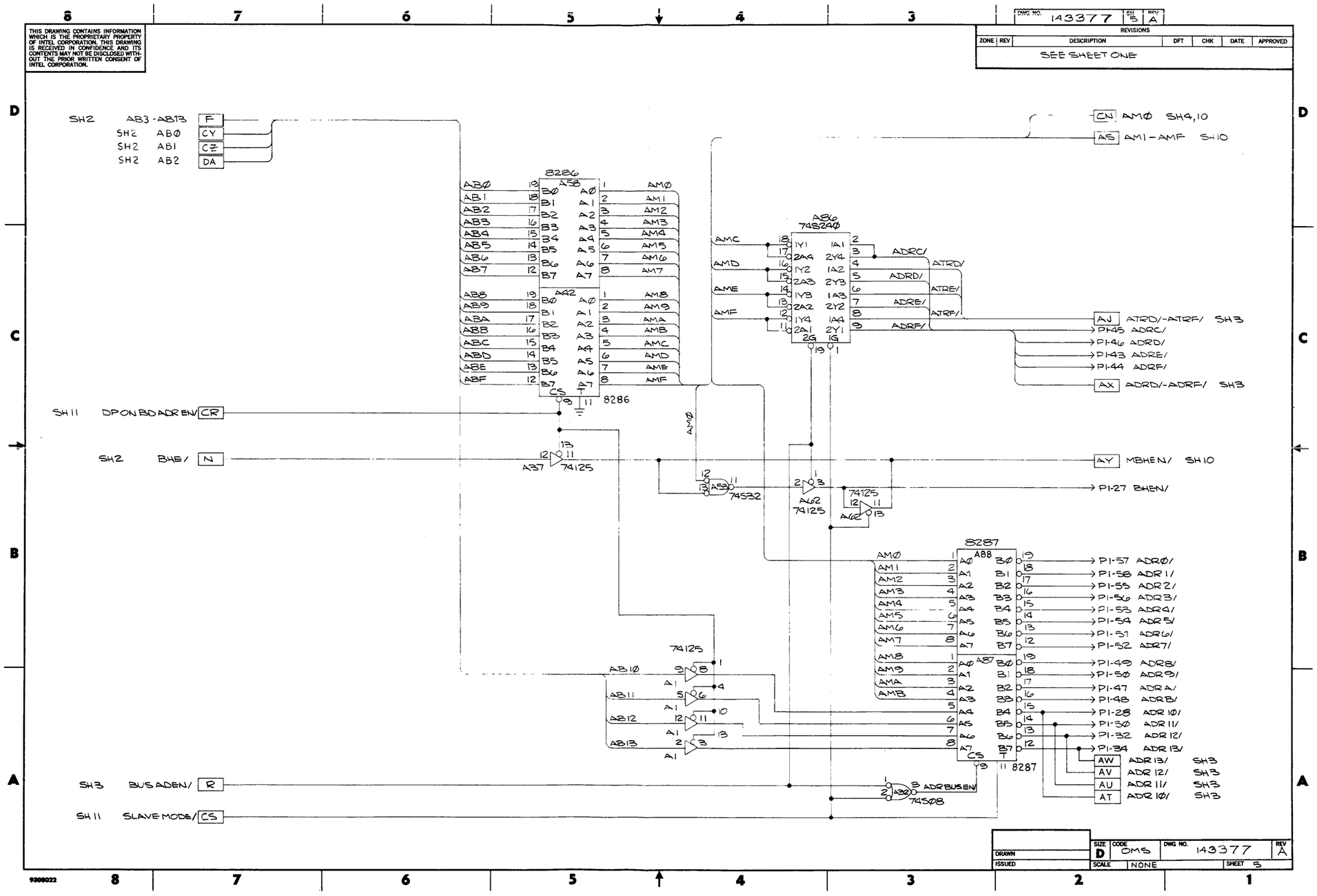
CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 4 of 11)

Glossary

ADR0-ADR13	Address 0-13
AM0-AMF	Memory Address 0-F
BHEN	Byte High Enable
MBHEN	Memory Byte High Enable





CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 5 of 11)

Jumpers

Jumpers	Factory Default	Option
E94-E96 E97-E99 S1	E94-E96 E97-E98 2716 Mode	See table 2-4

Glossary

8251 CS	8251 Chip Select
8253 CS	8253 Chip Select
8255 CS	8255 Chip Select
8259 CS	8259 Chip Select
DB0-DBF	Data Bus 0-F
IO AACK	Input/Output Advanced Acknowledge
ON BD ADR	On Board Address
ON BD RAM REQ	On Board Random Access Memory Request
PCS0	PROM Chip Select 0
PCS1	PROM Chip Select 1
PROM AACK	Programmable Advanced Acknowledge
PROM IO EN	Programmable Input/Output Enable

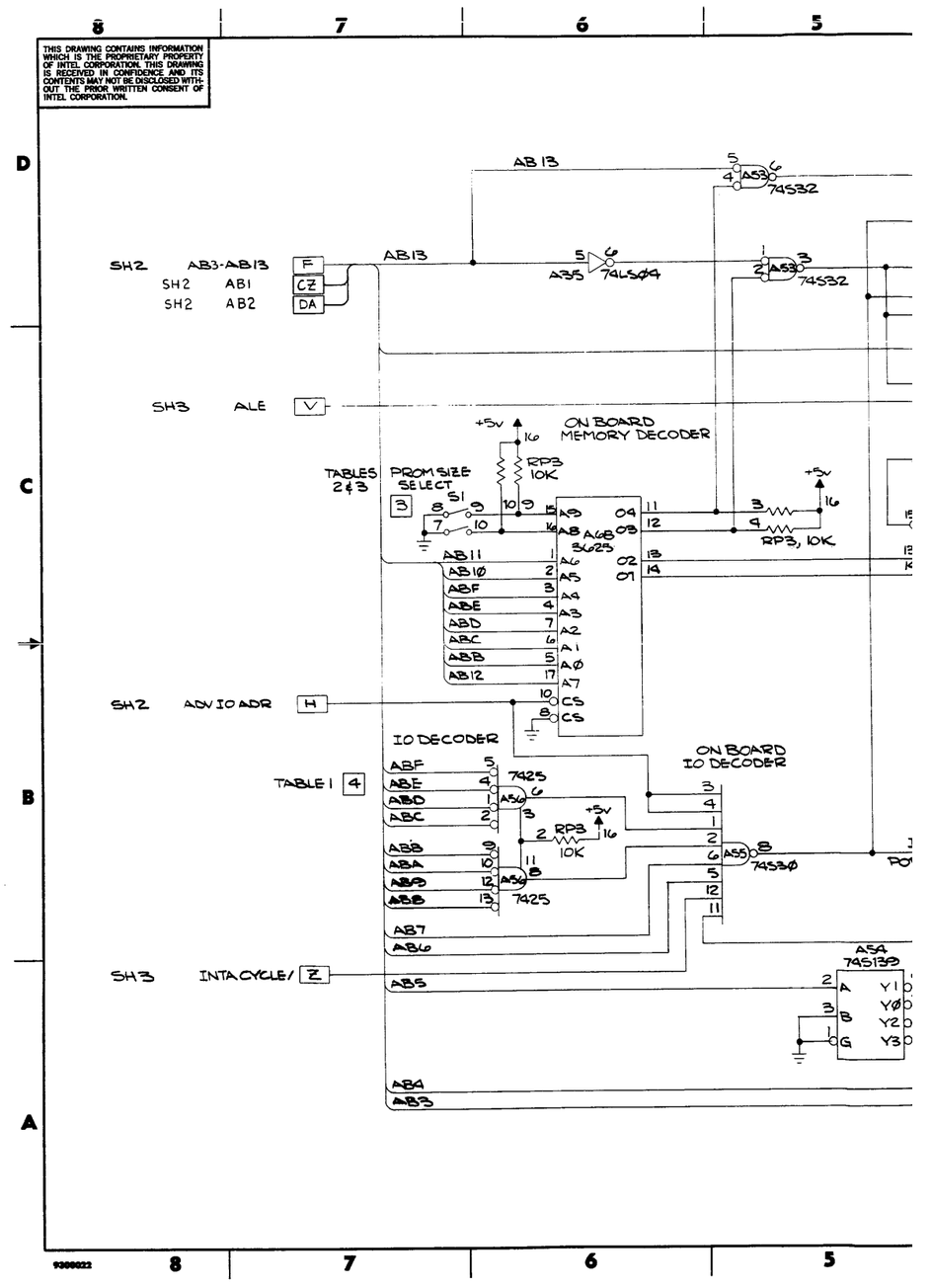


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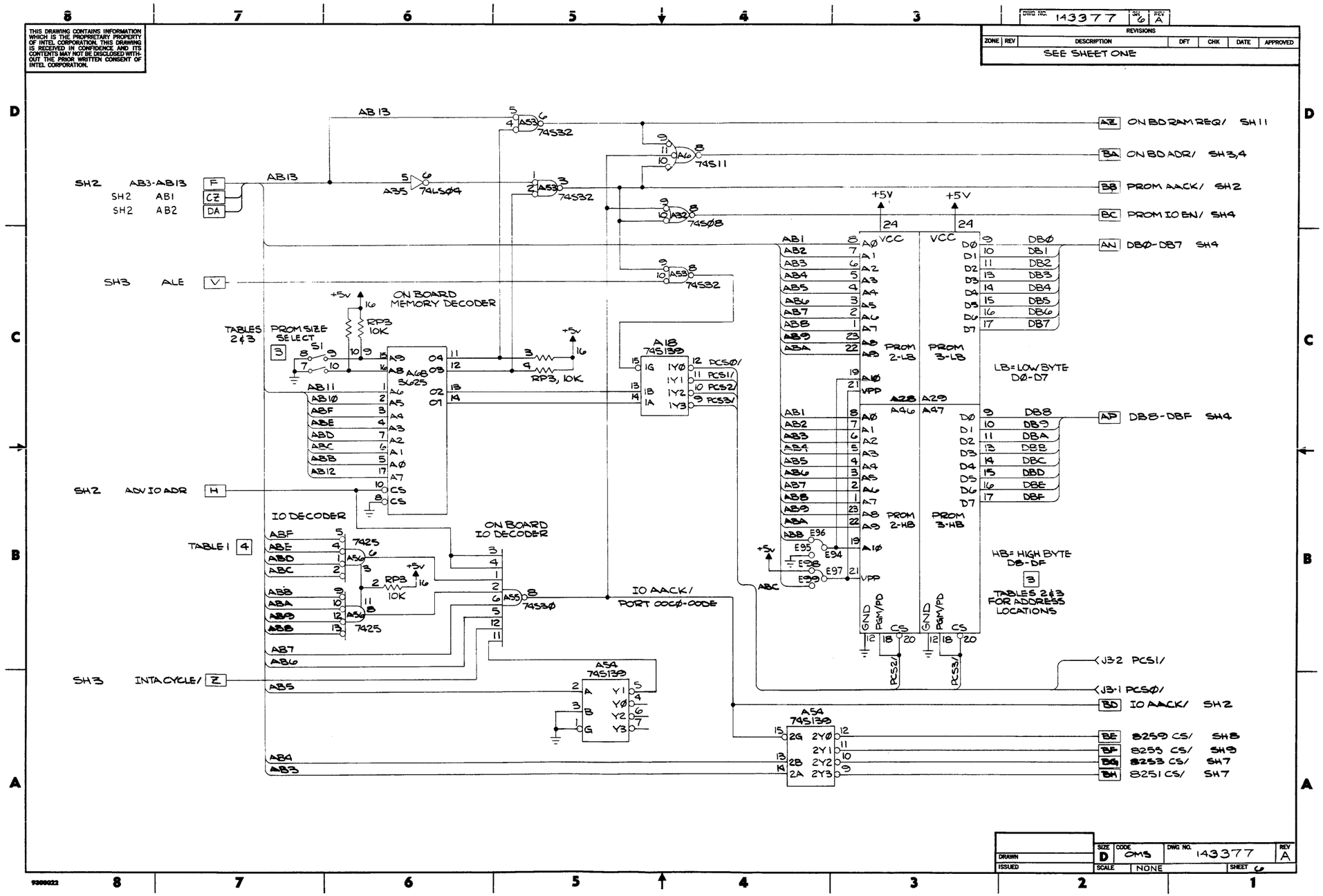
table 2-4



CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

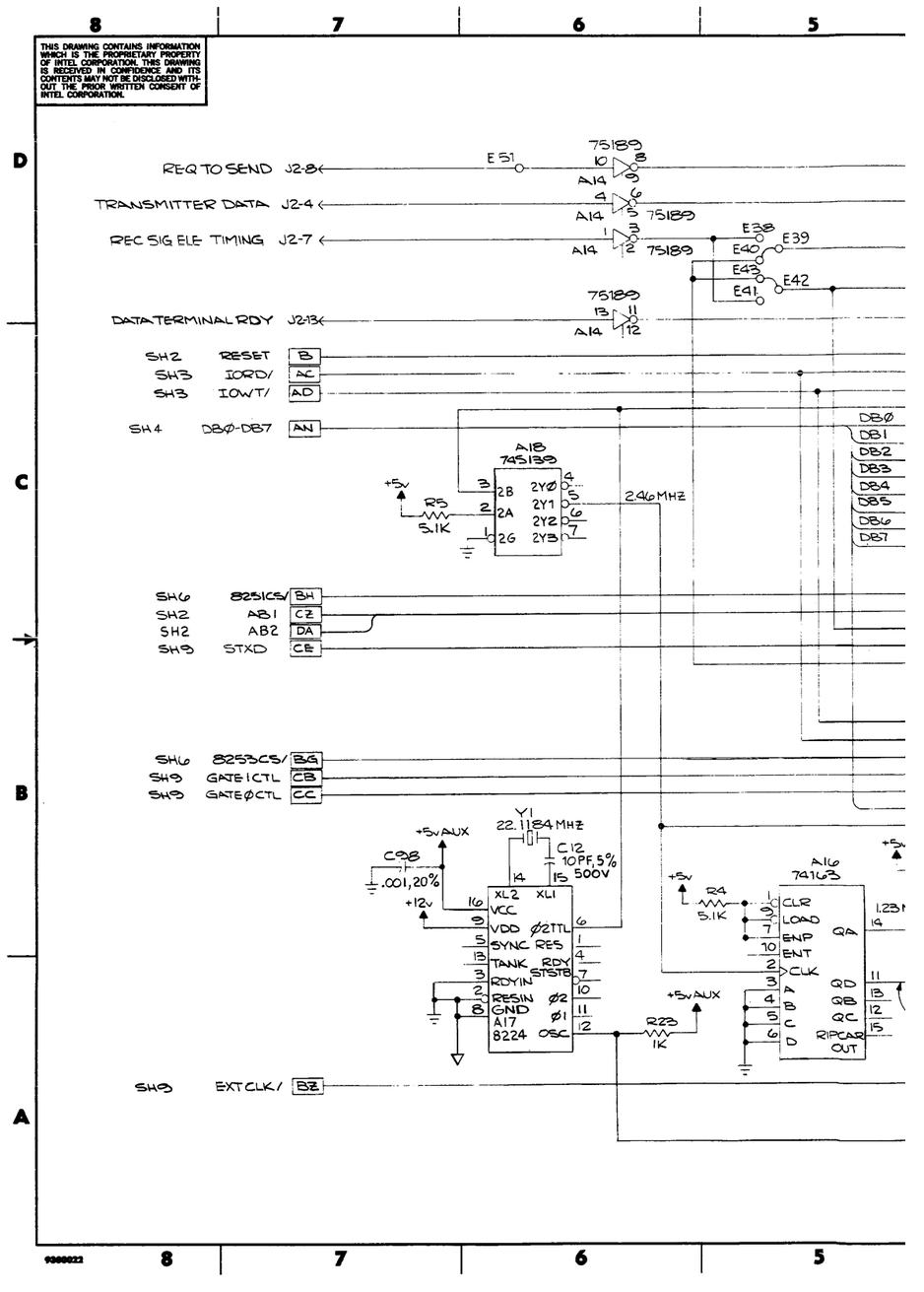
Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 6 of 11)

Jumpers

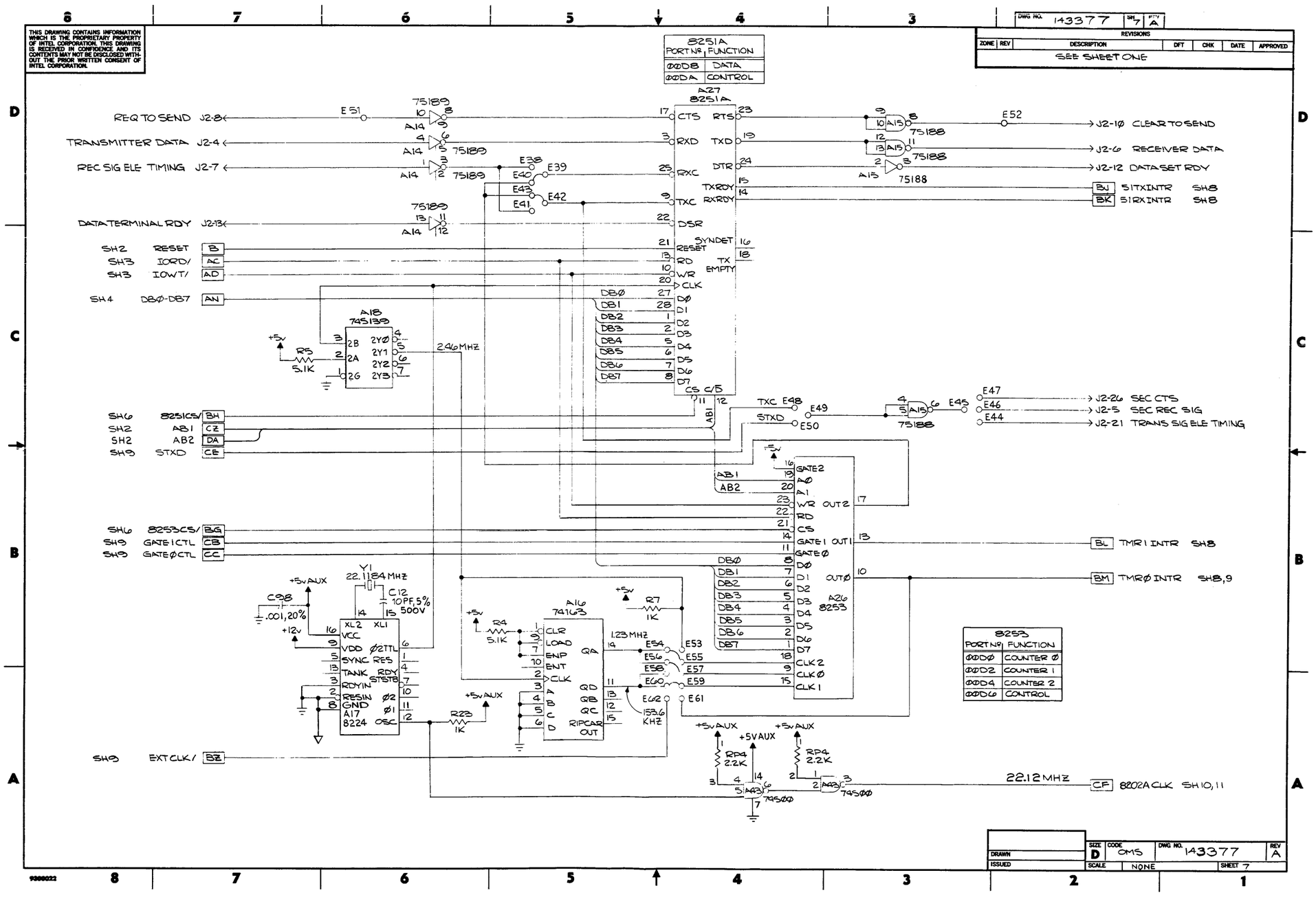
Jumpers	Factory Default	Option
E38-E40	E39-E40	See table 2-6
E41-E43	E42-E43	
E44-E47	Open	
E48-E50	Open	
E51-E52	Open	
E53-E55	E54-E55	See table 2-4
E56-E58	E56-E57	
E59-E62	E59-E60	

Glossary

51TX INTR	8251 Transmit Interrupt
51RX INTR	8251 Receive Interrupt
8202 CLK	8202 Clock
DATA SET RDY	Data Set Ready
SEC CTS	Secondary Clear to Send
SEC REC SIG	Secondary Receive Signal
TMR0 INTR	Timer 0 Interrupt
TMR1 INTR	Timer 1 Interrupt
TRANS SIG ELE TIMING	Transmit Signal Element Timing



Option
table 2-6
table 2-4



CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

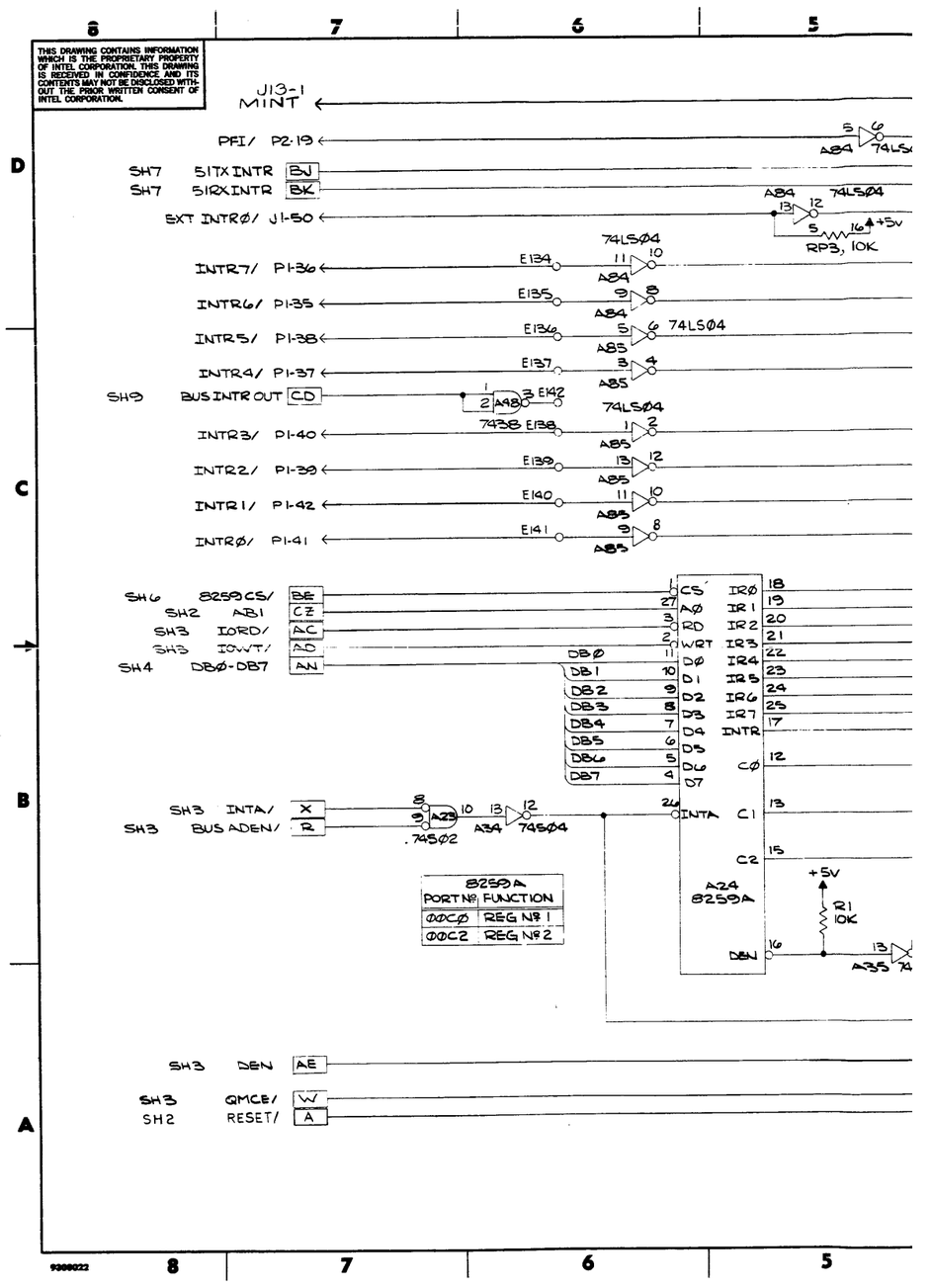
Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 7 of 11)

Jumpers

Jumpers	Factory Default	Option
E65-E91 E134-E142 87-89*	E68-E76, E79-E83 No Connection NMI Disable	See paragraph 2-14

Glossary

1st INTA DEN	First Interrupt Acknowledge Data Enable
BUS INTA DEN	Bus Interrupt Acknowledge Data Enable
INTR	Interrupt
Local INTA	Local Interrupt Acknowledge
Local INTA DE	Local Interrupt Acknowledge Data Enable
NMI	Non-maskable Interrupt
PA INTR	Port A Interrupt
PB INTR	Port B Interrupt



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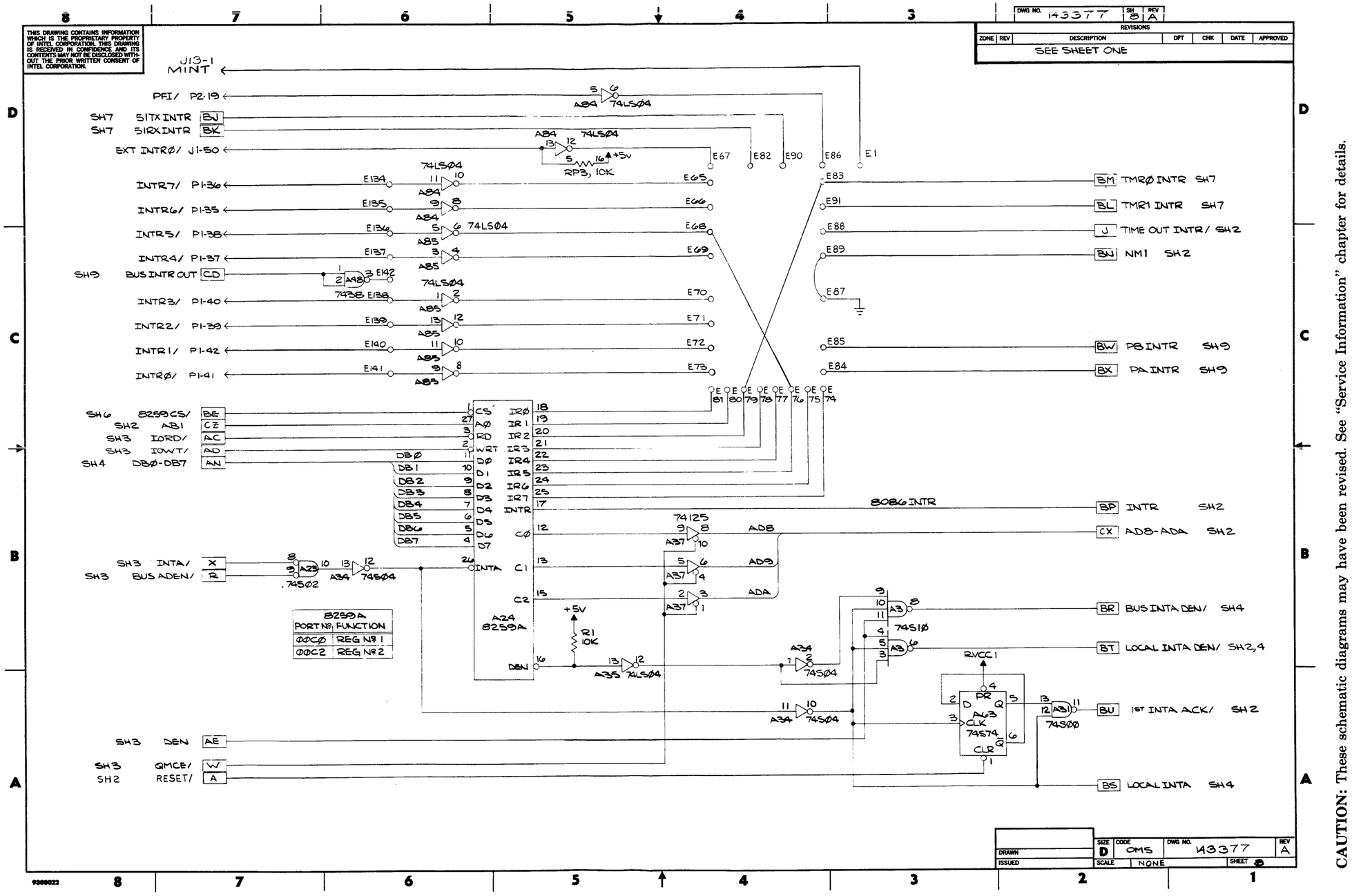


CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

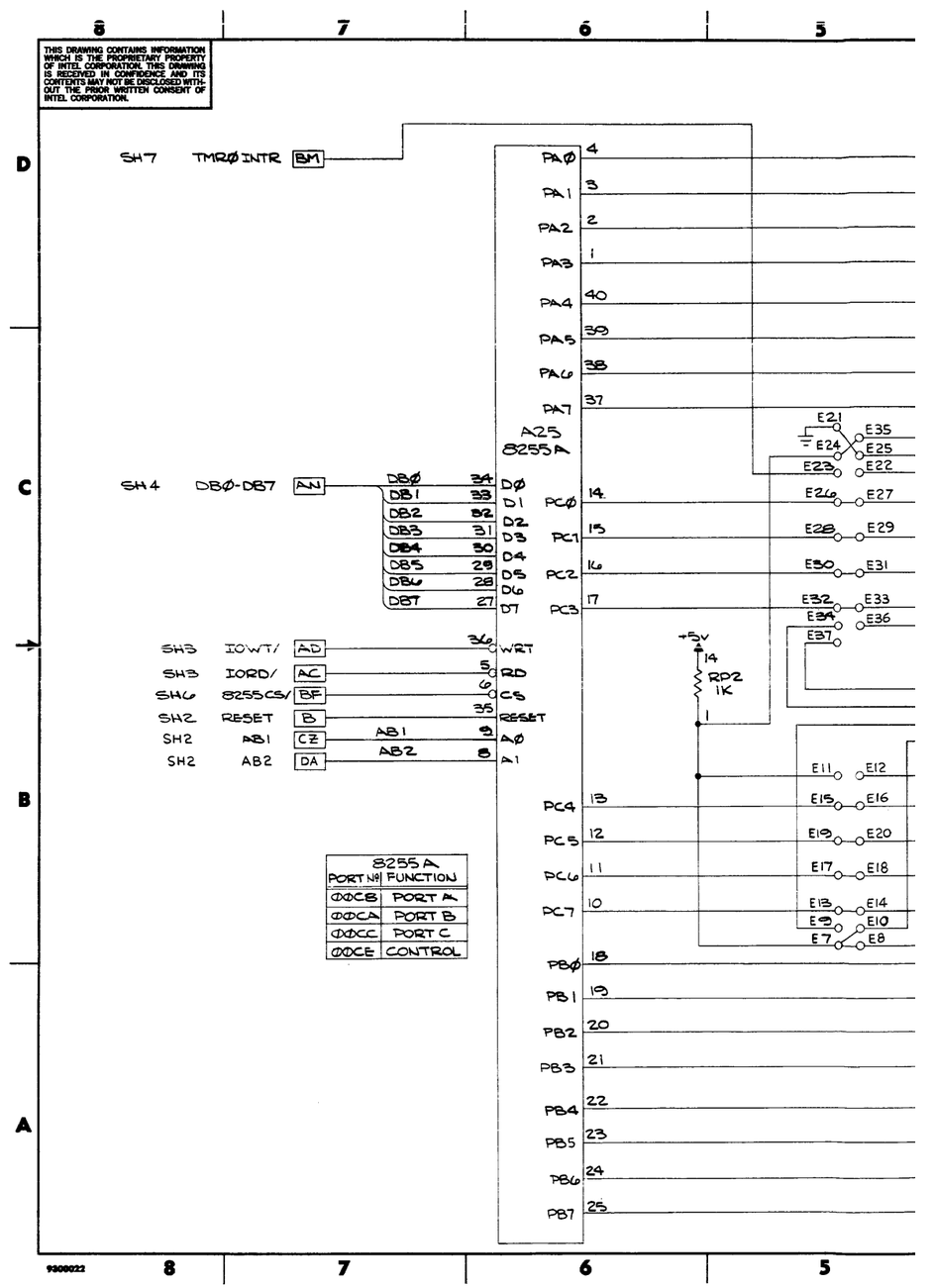
Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 8 of 11)

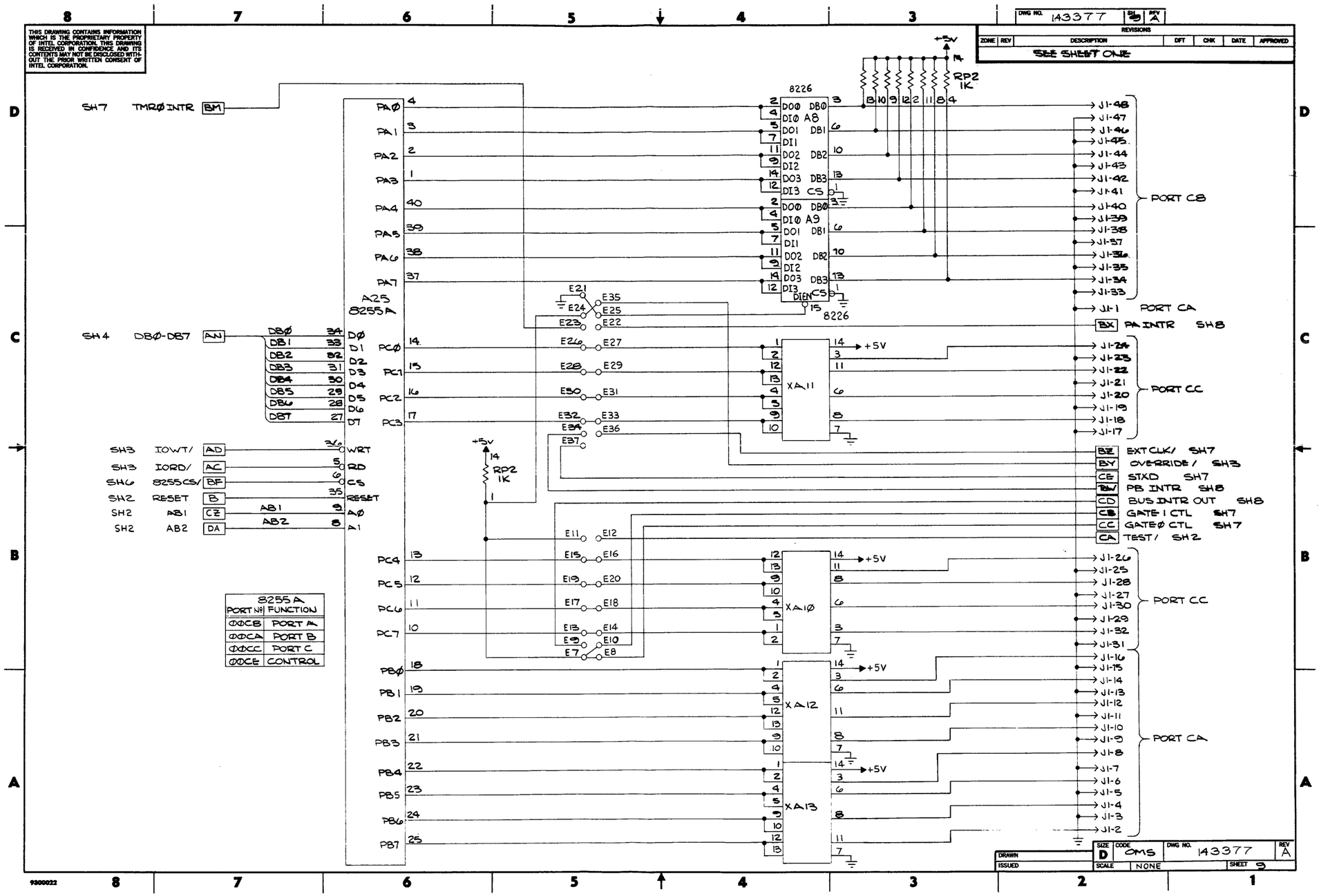
Jumpers

Jumpers	Factory Default	Option
E7-E20 E21-E37	E7-E8, E7-E10, E13-E14, E17-E18, E19-E20, E15-E16 E21-E25, E24-E35, E26-E27, E28-E29, E30-E31, E32-E33	See paragraph 2-16

Glossary

BUS INTR OUT	Bus Interrupt Out
EXT CLK	External Clock
GATE 0 CTL	Gate 0 Control
GATE 1 CTL	Gate 1 Control
STXD	Secondary Transmit Data





CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

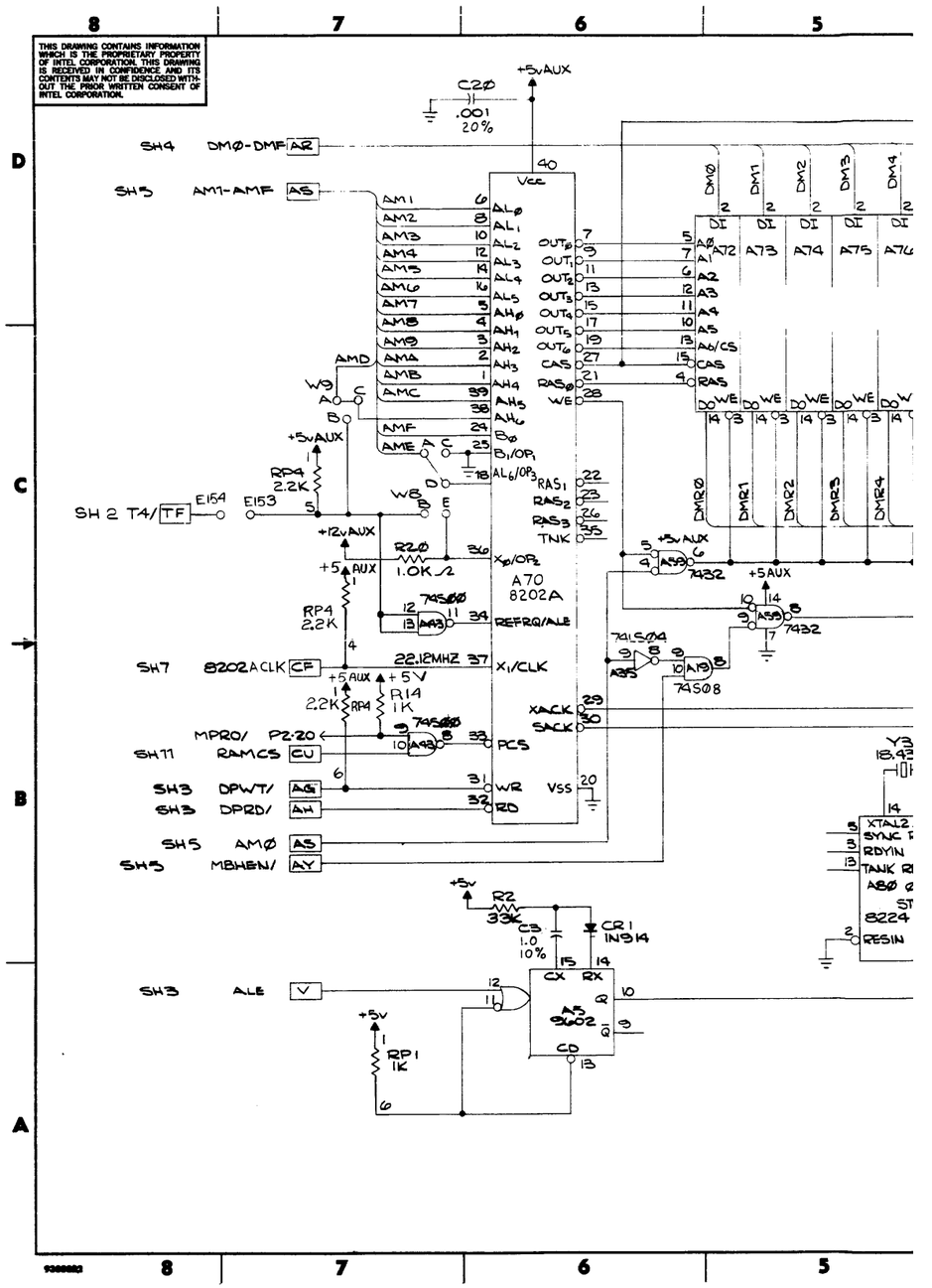
Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 9 of 11)

Jumpers

Jumpers	Factory Default	Option
E103-E104 E105-E106 W8 A-D W9 A-C	Installed Installed Installed Installed	See table 2-9

Glossary

BCLK	Bus Clock
CAS	Column Address Strobe
CCLK	Constant Clock
DMR0-DMRF	Dynamic RAM Output 0-F
RAM AACK	Random Access Memory Advance Acknowledge
RAM XACK	Random Access Memory Transfer Acknowledge
WE1-WE2	Write Enable 1 and 2



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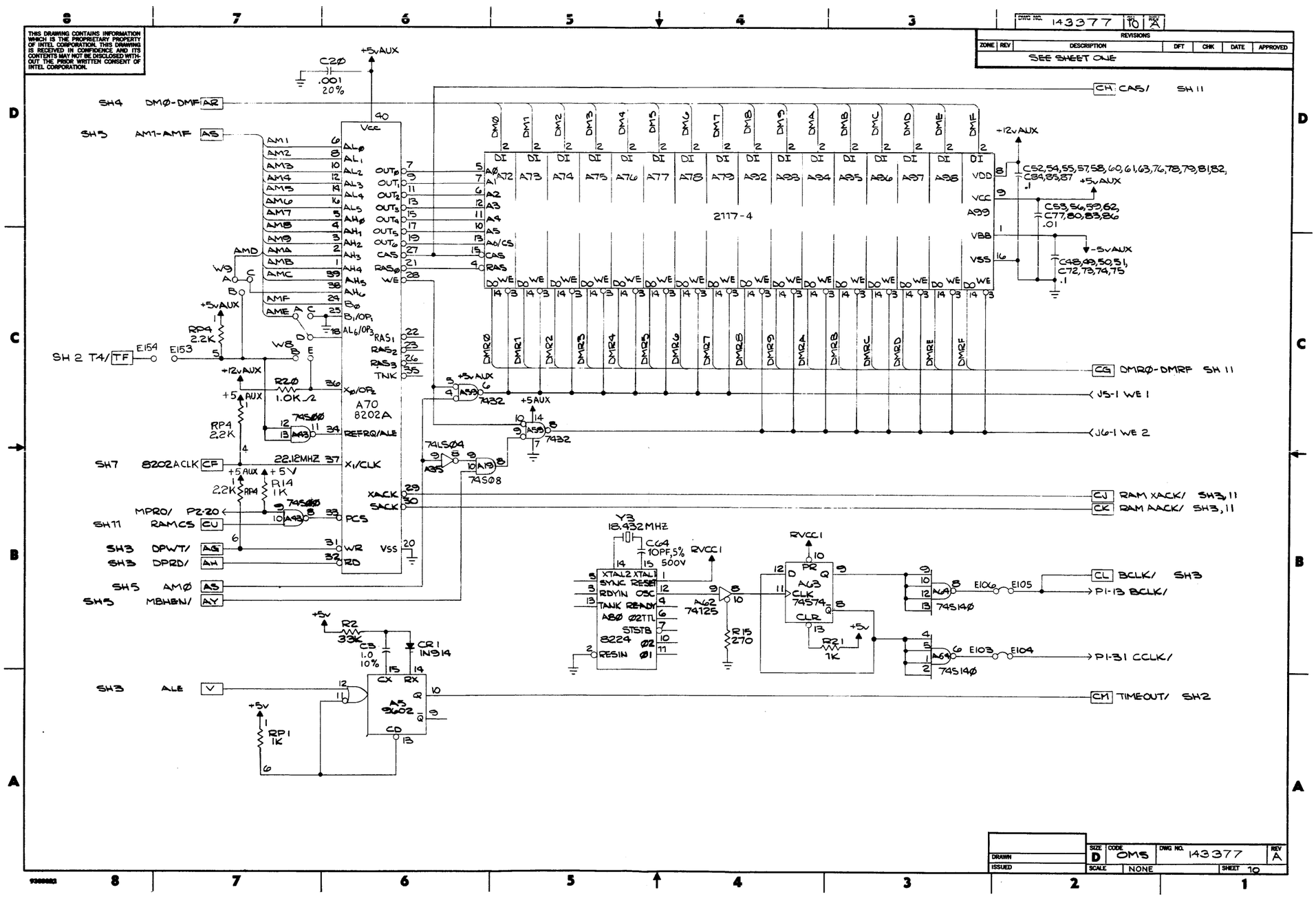
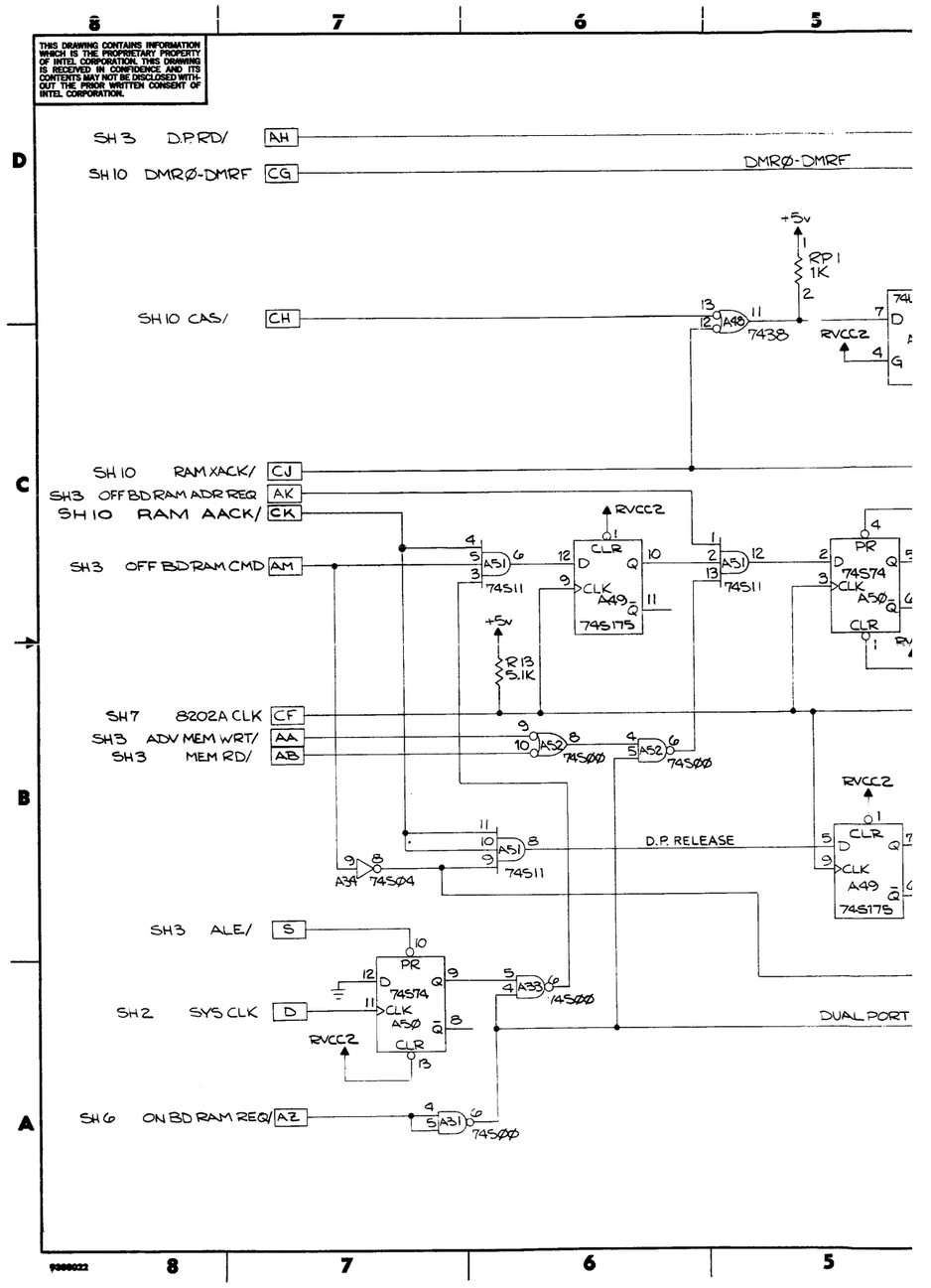


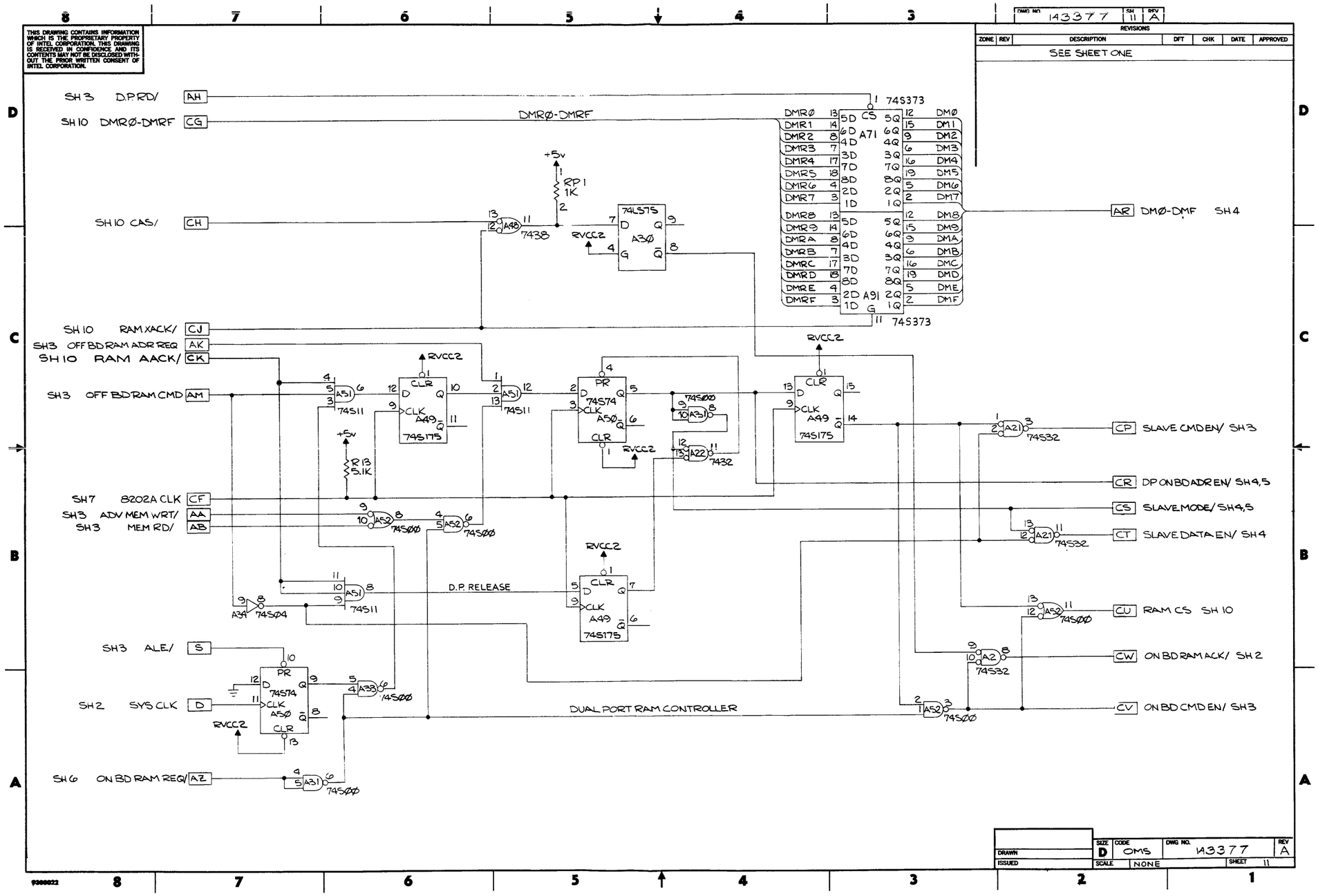
CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 10 of 11)

Glossary

DP ON BD ADR EN	Dual Port On Board Address Enable
ON BD CMD EN	On Board Command Enable
ON BD RAM ACK	On Board Random Access Memory Acknowledge
RAM CS	Random Access Memory Chip Select
SLAVE CMD EN	Slave Command Enable
SLAVE DATA EN	Slave Data Enable





CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-2. iSBC 86/12A Schematic Diagram (Sheet 11 of 11)